

US-PAT-NO: 6077726

DOCUMENT-IDENTIFIER: US 6077726 A

TITLE: Method and apparatus for stress  
relief in solder bump  
formation on a semiconductor device

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Detailed Description Text - DETX (5):

Still referring to FIG. 1, an under bump metal (UBM) layer 18 is formed over the opening in polyimide layer 16 and covering polyimide layer 16 and metal pad 12. In the illustrated embodiment, UBM layer 18 is formed of nickel. In other embodiments, UBM layer 18 may be formed of any other type of metal. A thin gold layer 20 is formed over UBM layer 18 using an electroless plating process. Solder bump 22 is then formed over gold layer 20 using a stencil and solder paste. In the illustrated embodiment, solder bump 22 is a eutectic solder bump composed of approximately 63% tin and 37% lead. The solder paste is reflowed at a temperature of approximately 200.degree. C., forming solder bump 22.

Detailed Description Text - DETX (12):

The photomask used to limit the side growth of UBM layer 34 is removed and polyimide layer 36 is spun-on over passivation layer 14. Polyimide layer extends over UBM layer 34 by a distance labeled "d" in FIG. 3. The distance "d" is in the range of 3-12 microns in the illustrated embodiment. However, in other embodiments the distance "d" may be less than or greater than 3-12 microns. Solder bump 38 is then either stencil printed,

electroplated, or  
evaporated onto the exposed area of UBM layer 34 using  
conventional techniques.  
By extending polyimide layer 36 over UBM layer 34, the  
metal layers are  
separated from passivation layer 14, thus preventing any  
cracks when may  
develop from propagating in passivation layer 14 and also  
preventing cratering  
of semiconductor material 10.

Claims Text - CLTX (14):

10. The method as in claim 9, wherein the eutectic  
solder bump is formed  
using a stencil and solder paste.